ABSTRACT OF THE DISCLOSURE

A method and apparatus for a microprocessor with a divided register alias table is disclosed. In one embodiment, a first register alias table may have a full set of read and write ports, and a second register alias table may have a smaller set of read and write ports. The second register alias table may include translations for those logical register addresses that are used less frequently. When the second register alias table is called upon to translate more logical register addresses than it has read ports, in one embodiment a pipeline stall may permit additional time to utilize the limited read ports. In another embodiment, additional build rules for a trace cache may be utilized.